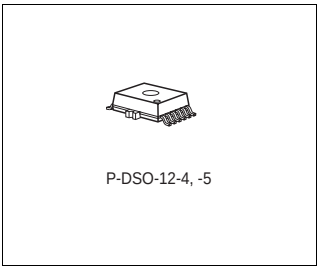
Dual Low Drop Voltage Regulator

TLE 7469

Features



- Dual output
  5 V (±2%), 320mA and 2.6 V[1] (±4%), 300mA or
  5 V (±2%), 320mA and 3.3 V (±3%), 300mA
- Ultra low quiescent current consumption < 55 µA
- Inhibit function
- Very low dropout voltage
- Reset with power-on delay
- Early Warning comparator
- Window watchdog
- Power sequencing for dual voltage µC
- Output protected against short circuit
- Wide operation range: up to 45 V
- Wide temperature range: -40 °C to 150 °C
- Overtemperature protection
- Overload protection

Functional Description

The TLE 7469 is a monolithic integrated voltage regulator with two voltage outputs specially designed to supply microcontrollers with dual supply voltage: 2.6 V[1] or 3.3 V core and 5 V I/O voltage like the Infineon XC164 and XC161.

1) 2.5 V nominal specification range of most µCs is compatible with the 2.6 V output voltage range of the TLE 7469.

Type	Ordering Code	Package
TLE 7469 GV52	Q67007-A9689	P-DSO-12-4
TLE 7469 GV53	Q67007-A9690	P-DSO-12-4

The voltage regulator features an integrated reset circuitry which monitors the 2.6 V/ 3.3 V supply voltage. At power on the reset checks both supply voltages and performs the power-on reset with an adjustable delay time. The voltage difference is kept in the range -0.5 V < (V_{Q1} - V_{Q2}) < 3.0 V even during power-on and power-down time enabling save µC operation without external clamping. Using the integrated early warning comparator an external voltage can be supervised. An integrated output sink current circuitry keeps the voltage at the Q1 pin below 5.5 V even when reverse currents are applied. Thus connected devices are protected from overvoltage damage. The regulator can be shut down via the Inhibit input causing the current consumption to drop below 9 µA.

The TLE 7469 is designed for use under the severe conditions of automotive applications, and is therefore equipped with protection functions against overload, short circuit and overtemperature. It operates in the wide junction temperature range from -40 °C to 150 °C and offers the low quiescent current consumption required for body applications.

For applications requiring extremely low noise levels the Infineon voltage regulator family TLE 42XY and TLE 44XY is more suited than the TLE 7469. A mV-range output noise on the TLE 7469 caused by the charge pump operation is unavoidable due to the ultra low quiescent current concept.

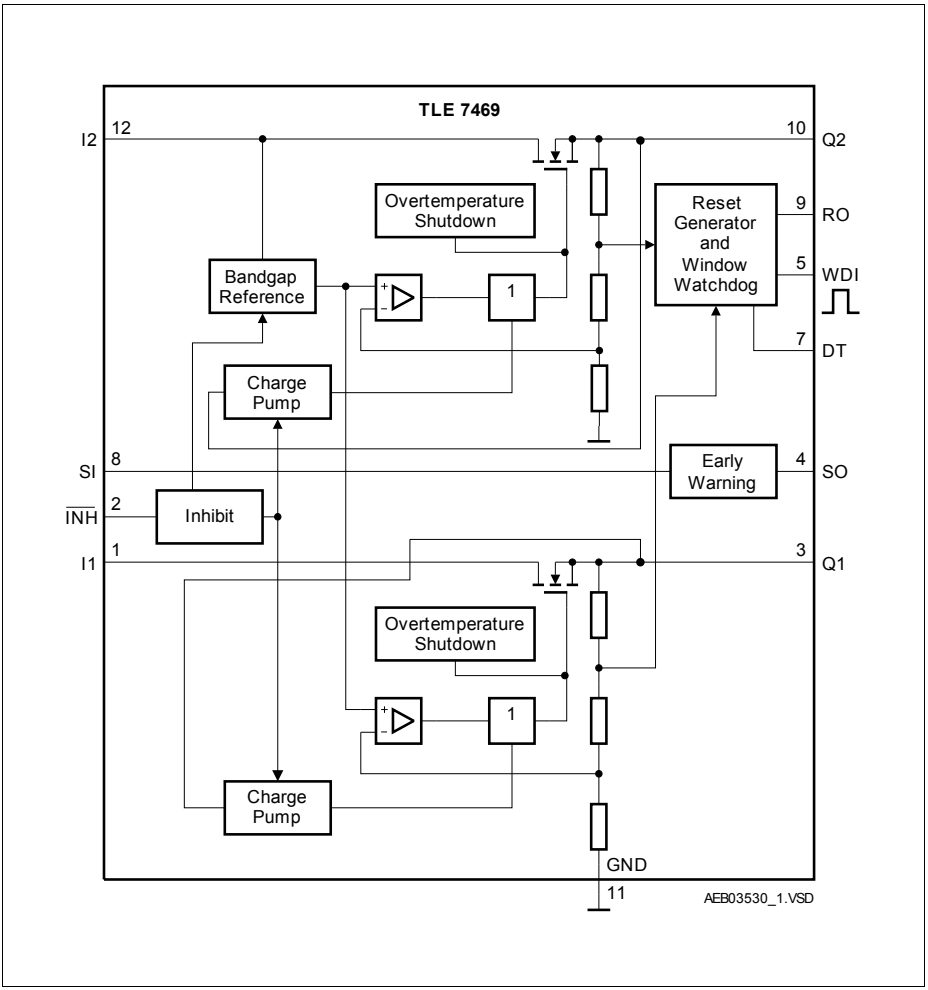


Figure 1 Block Diagram

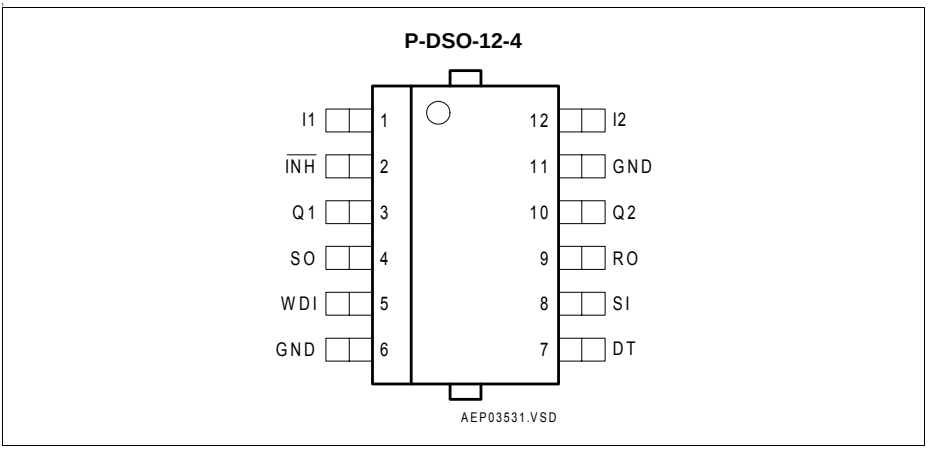


Figure 2 **Pin Configuration** (top view)

Table 1 **Pin Definitions and Functions**

Pin No.	Symb.	Function
1	I1	**Input voltage 1;** block to ground directly at the IC with a 100 nF ceramic capacitor
2	$\overline{\text{INH}}$	**Inhibit Input;** low level disables the IC. Integrated pull-down resistor
3	Q1	**Output voltage 1;** 5.0 V, block to GND with a capacitor $C_{Q1} \geq 1$ µF, ESR < 6 Ω at 10 kHz
4	SO	**Sense output;** Output of Early Warning Comparator, open collector output
5	WDI	**Watchdog Input;** Trigger Input for Watchdog pulses
6, 11	GND	**Ground;** Pin 6, 11 and heat slug must be connected to GND
7	DT	**DT Delay timing;** connect to GND, Q1 or Q2 to select Reset and Watchdog timing
8	SI	**Sense input;** Input for Early Warning comparator
9	RO	**Reset output;** open collector output with integrated 20 kΩ pull-up resistor
10	Q2	**Output voltage 2;** 2.6 V (TLE 7469 GV52), 3.3 V (TLE 7469 GV53); block to GND with a capacitor $C_{Q2} \geq 1$ µF, ESR < 6 Ω at 10 kHz
12	I2	**Input voltage 2;** block to ground directly at the IC with a 100 nF ceramic capacitor

Table 2 Absolute Maximum Ratings

-40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input I1					
Voltage	V_{I1}	-0.3	45	V	–
Current	I_{I1}	–	–	mA	Internally limited
Input I2					
Voltage	V_{I2}	-0.3	45	V	–
Current	I_{I2}	–	–	mA	Internally limited
Output Q1					
Voltage	V_{Q1}	-0.3	5.5	V	Permanent
Voltage	V_{Q1}	-0.3	6.2	V	t < 10 s[1)]
Current	I_{Q1}	–	2	mA	Internally limited
Output Q2					
Voltage	V_{Q2}	-0.3	5.5	V	Permanent
Voltage	V_{Q2}	-0.3	6.2	V	t < 10 s[1)]
Current	I_{Q2}	–	–	mA	Internally limited
Inhibit Input $\overline{\text{INH}}$					
Voltage	$V_{\overline{\text{INH}}}$	-0.3	45	V	Observe current limit $I_{\overline{\text{INH}}\text{max}}$[2)]
Current	$I_{\overline{\text{INH}}}$	-1	1	mA	–
Reset Output RO					
Voltage	V_{RO}	-0.3	5.5	V	Permanent
Voltage	V_{RO}	-0.3	6.2	V	t < 10 s[1)]
Current	I_{RO}	–	–	mA	internally limited
Delay Timing DT					
Voltage	V_{DT}	-0.3	5.5	V	Permanent
Voltage	V_{DT}	-0.3	6.2	V	t < 10 s[1)]
Current	I_{DT}	-5	5	mA	–

Table 2 Absolute Maximum Ratings (cont'd)

-40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Watchdog Input WDI					
Voltage	V_{WDI}	-0.3	5.5	V	Permanent
Voltage	V_{WDI}	-0.3	6.2	V	t < 10 s[1)]
Current	I_{WDI}	–	–	mA	internally limited
Sense Input SI					
Voltage	V_{SI}	-0.3	45	V	Observe current limit I_{SImax}[2)]
Current	I_{SI}	-1	1	mA	–
Sense Output SO					
Voltage	V_{SO}	-0.3	5.5	V	Permanent
Voltage	V_{SO}	-0.3	6.2	V	t < 10 s[1)]
Current	I_{SO}	–	–	mA	internally limited
Temperatures					
Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

1) Exposure to these absolute maximum ratings for extended periods (t > 10 s) may affect device reliability.

2) External resistor required to keep current below absolute maximum rating when voltages ≥ 5.5 V are applied.

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. Integrated protection functions are designed to prevent IC destruction under fault conditions. Fault conditions are considered as outside normal operating range. Protections functions are not designed for continuous repetitive operation.

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	V_{I1}	5.6	45	V	–
Input voltage	V_{I2}	6.0	45	V	V_{I1} > 8V
Input voltage	V_{I2}	4.2	45	V	V_{I1} < 8V
Junction temperature	T_j	-40	150	°C	–
Thermal Resistances P-DSO-12-4					
Junction case	R_{thjc}	–	4.4	K/W	–
Junction ambient	R_{thj-a}	–	107	K/W	PCB, only Footprint[1)]
Junction ambient	R_{thj-a}	–	58	K/W	PCB Heat Sink Area 300 mm^2 [1)]
Junction ambient	R_{thj-a}	–	48	K/W	PCB Heat Sink Area 600 mm^2 [1)]

1) Package mounted on PCB 80 × 80 × 1.5 mm^3; 35µ Cu; 5µ Sn; zero airflow; 85 °C ambient temperature.

Note: In the operating range the functions given in the circuit description are fulfilled.

Table 4 Electrical Characteristics

V_{I1} = 13.5 V; V_{I2} = 13.5 V; -40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Output Q1						
Output voltage	V_{Q1}	4.90	5.0	5.10	V	1 mA < I_{Q1} < 215 mA, 6 V < V_{I1} < 16 V
Output current limitation	I_{Q1}	320	–	700	mA	V_{Q1} = 4.0 V
Output drop voltage; V_{DRQ1} = V_{I1} - V_{Q1}	V_{DRQ1}	–	300	600	mV	I_{Q1} = 215 mA[1)]
Load regulation	$\Delta V_{Q1,Lo}$	–	25	60	mV	1 mA < I_{Q1} < 215 mA
Line regulation	$\Delta V_{Q1,Li}$	–	20	50	mV	I_{Q1} = 1 mA, 10 V < V_I < 28 V
Power Supply Ripple Rejection	$PSRR$	–	60	–	dB	f_r = 100 Hz, V_r = 1 Vpp
Reverse Output Current Protection	$V_{Q,REV}$	–	–	5.5	V	$I_{Q,REV}$ = 1 mA, $V_{\overline{INH}}$ = 0 V
Output Q2						
Output voltage	V_{Q2}	2.50	2.60	2.70	V	1 mA < I_{Q2} < 200 mA, 6 V < V_{I2} < 16 V, TLE 7469 GV52
Output voltage	V_{Q2}	3.20	3.30	3.40	V	1 mA < I_{Q2} < 200 mA, 6 V < V_{I2} < 16 V, TLE 7469 GV53
Absolute differential voltage	V_{Q1} - V_{Q2}	-0.5	–	3.0	V	V_{Q1}, V_{Q2} > 1 V
Output current limitation	I_{Q2}	300	–	500	mA	V_{Q2} = 2.0 V
Load regulation	$\Delta V_{Q2,Lo}$	–	25	60	mV	1 mA < I_{Q2} < 200 mA
Line regulation	$\Delta V_{Q22,Li}$	–	20	50	mV	I_{Q2} = 1 mA, 10 V < V_I < 28 V
Power Supply Ripple Rejection	$PSRR$	–	60	–	dB	f_r = 100 Hz, V_r = 1 Vpp

Table 4 Electrical Characteristics (cont'd)

V_{I1} = 13.5 V; V_{I2} = 13.5 V; -40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Current Consumption						
Quiescent current; $I_q = I_{I1} + I_{I2} - I_{Q1} - I_{Q2}$	I_q	–	–	55	µA	$I_{Q2} = I_{Q1}$ = 100 µA, T_j < 80 °C
Quiescent current; inhibited	I_q	–	5	9	µA	$V_{\overline{INH}}$ = 0 V, T_j < 80 °C
Inhibit Input $\overline{INH}$						
Turn-on Voltage	$V_{\overline{INH}\ ON}$	–	–	3.1	V	V_{Q1} & V_{Q2} on
Turn-off Voltage	$V_{\overline{INH}\ OFF}$	0.8	–	–	V	V_{Q1} & V_{Q2} off
H-input current	$I_{\overline{INH}\ ON}$	–	3	4	µA	$V_{\overline{INH}}$ = 5 V
L-input current	$I_{\overline{INH}\ OFF}$	–	0.5	1	µA	$V_{\overline{INH}}$ = 0 V, T_j < 80 °C
Delay Timing DT						
Threshold Fast Timing Select	$V_{DT,FAST}$	4.5	–	–	V	–
Threshold Slow Timing Select	$V_{DT,SLOW}$	2.3	–	3.3	V	TLE 7469 GV52
Threshold Slow Timing Select	$V_{DT,SLOW}$	2.3	–	3.6	V	TLE 7469 GV53
Threshold Watchdog Turn Off[2)]	$V_{DT,OFF}$	–	–	0.8	V	–
Watchdog Input WDI						
H-input voltage threshold	V_{WDIH}	–	–	3.0	V	–
L-input voltage threshold	V_{WDIL}	–	–	0.8	V	–
Watchdog sampling time	t_{sam}	0.20	0.25	0.30	ms	Fast Timing
		0.80	1.00	1.20	ms	Slow Timing
Ignore window time	t_{OW}	25.6	32.0	38.4	ms	Fast Timing
		102	128	154	ms	Slow Timing
Open window time	t_{OW}	25.6	32.0	38.4	ms	Fast Timing
		102	128	154	ms	Slow Timing

Table 4 Electrical Characteristics (cont'd)

V_{I1} = 13.5 V; V_{I2} = 13.5 V; -40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Closed window time	t_{CW}	25.6	32.0	38.4	ms	Fast Timing
		102	128	154	ms	Slow Timing
Window watchdog trigger time	t_{WD}	39.0	44.8	50.6	ms	Fast Timing
		156	179	202	ms	Slow Timing
Reset Output RO						
Reset switching threshold 2	V_{RT2}	2.35	2.38	2.48	V	TLE 7469 GV52, V_{Q2} decreasing
Reset Headroom 2	V_{RH2}	130	190		mV	TLE 7469 GV52
Reset switching threshold 2	V_{RT2}	3.00	3.07	3.15	V	TLE 7469 GV53, V_{Q2} decreasing
Reset Headroom 2	V_{RH2}	165	240		mV	TLE 7469 GV53
Reset hysteresis 2	V_{RH2}	–	45	–	mV	TLE 7469 GV52 [3]
		–	60	–	mV	TLE 7469 GV53 [4]
Reset switching threshold 1	V_{RT1}	4.50	4.65	4.80	V	V_{Q1} decreasing
Reset hysteresis 1	V_{RH1}	–	90	–	mV	–
Reset sink current	I_{RO}	–	–	1	mA	V_Q = 5 V, V_{RO} = 0.5 V
Reset output low voltage	V_{ROL}	–	0.15	0.25	V	$V_{Q2} \geq 1$ V
Reset high voltage	V_{ROH}	4.5	–	–	V	–
Integrated reset pull-up resistor	R_{RO}	10	20	40	kΩ	Internally connected to Q1
Power-up Reset delay time	T_{RD}	6.0	8.0	10.0	ms	Fast Timing ($V_{DT} \geq 4.5$ V)
		24.0	32.0	40	ms	Slow Timing ($V_{DT} \leq 3.3$ V)
Reset Reaction Time	T_{RR}	–	10	26	µs	–

Table 4 Electrical Characteristics (cont'd)

V_{I1} = 13.5 V; V_{I2} = 13.5 V; -40 °C < T_j < 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage Sense						
Sense threshold high	V_{SIH}	1.10	1.16	1.22	V	V_{SI} increasing (see **Figure 4**)
Sense threshold low	V_{SIL}	1.06	1.12	1.18	V	V_{SI} decreasing (see **Figure 4**)
Sense output low voltage	V_{SOL}	–	0.1	0.4	V	V_{SI} < 1.01 V; V_{I1} > 4.20 V; I_{SO} = 0.5 mA
External SO pull-up resistor	$R_{SO\ ext}$	9.2	–	–	kΩ	V_{Q1} = 5V
Sense input current	I_{SI}	-1	0.1	1	µA	V_{SI} = 5 V
Sense high reaction time	$t_{pd\ SO\ LH}$	–	4.0	–	µs	–
Sense low reaction time	$t_{pd\ SO\ HL}$	–	4.0	–	µs	–

1) Measured when the output voltage has dropped 100 mV from the nominal Value obtained at V_{I1} = 13.5 V, V_{I2} = 13.5 V.

2) Watchdog off, Reset in slow mode.

3) Specified by design, not subject of production test.

4) Specified by design, not subject of production test.

Application Information

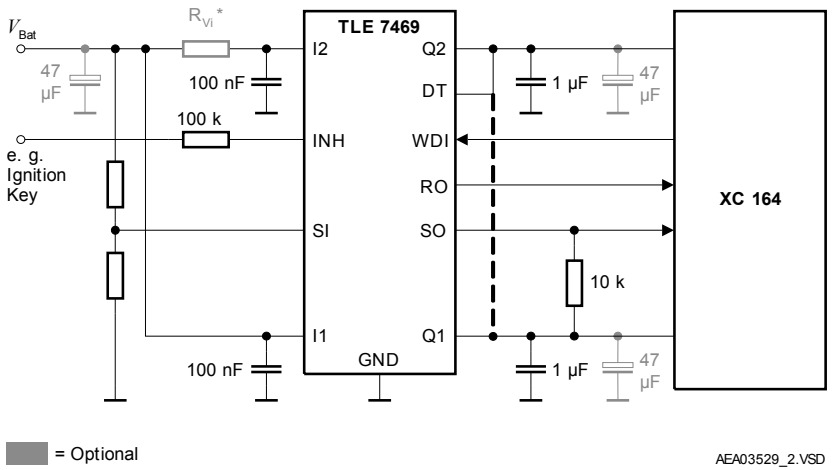


Figure 3 Application Diagram with Typical External Components

A typical application of the TLE 7469 is shown in **Figure 3**. To prevent the regulation loop from oscillating a ceramic capacitor of $C_{Q1/2} \geq 1$ µF is required at each of the outputs Q1 and Q2. In contrast to most low drop voltage regulators the TLE 7469 only needs moderate capacitance at the outputs and tolerates ceramic capacitors to keep the stability. This offers more design flexibility to the circuit designer enabling also to operate the device without tantalum capacitors.

Additional a capacitor C_B of 10 … 47 µF should be used for each output Q1 and Q2 to suppress influences from load surges to the voltage levels. This one can either be an aluminum electrolytic capacitor or a tantalum capacitor following the application requirements.

General recommendation at Tj<90°C is to keep the drop over the equivalent serial resistor (ESR) together with the discharge of the blocking capacitor below 300mV. Since the regulator output current roughly rises linearly with time the discharge of the capacitor can be calculated as:

$$dVC_B = dI_Q * dt / C_B$$

The drop across the ESR calculates as:

DVESR = DI*ESR (5.2)

To prevent a reset the following relationship must be fullfilled:

DVC + DVESR < 300mV (5.3)

Example: let us assume we have a load current change of 100mA and a blocking capacitor of 22µF.

DVC = 0.1A * 25µs/22µF = 114mV

So for the ESR we can allow

DVESR = 300mV - 114mV = 186mV

The permissible ESR becomes:

ESR = 186mV/100mA = 1.86Ohm

As a dual regulator the TLE 7469 for correct operation should be always supplied at both input pins I1 and I2 out of one voltage supply. The dual voltage regulator with both inputs accessible, offers the possibility to reduce the power dissipation in the package. This can be achived by two different input voltages or a Drop Resistor* R_{Vi} (see **Figure 3**) at the input pin I2 for the 2.6V output. If one of this options is chosen,care should be taken, to apply the device as descibet under “Table 3: Operating Range”.

The reset output RO features an integrated pull-up resistor. Thus it can be directly coupled to the microcontroller reset input.

The sense comparator output SO is an open collector. An appropriate external pull-up resistor is typ. 5.6 kΩ … 47 kΩ, the minimum value of 5.6 kΩ being defined by the max. sink current capability of the SO output transistor. If the sense comparator is not used of course the pull-up resistor can be spared. In this case the SI pin should be directly connected to Q1 in order to keep the comparator inactive.

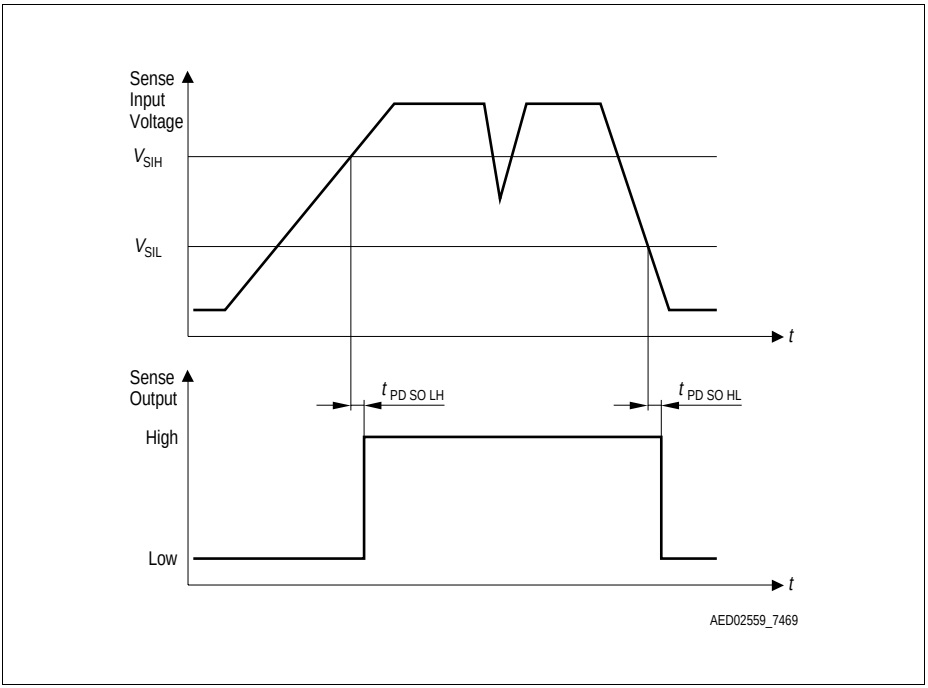


Figure 4 Sense Timing Diagram

Circuit Description

Power On Reset

In order to avoid any system failure, a sequence of several conditions has to be passed. When the level of V_{Q2} reaches the reset threshold V_{RT}, the signal at RO remains LOW for the Power-up reset delay time T_{RD}. Then a second comparator checks whether $V_{Q1} \geq V_{RT1}$ and only if this test is passed the reset output is switched to HIGH. The Reset output is only released (set to High level) if both output voltages have passed their specific reset threshold $V_{RT1/2}$. The reset function and timing is illustrated in **Figure 5**.

The reset reaction time T_{RR} avoids wrong triggering caused by short “glitches” on the V_{Q2}-line. For power-fail, in case of V_{Q2} or V_{Q1} power down ($V_{Q2} < V_{RT2}$ or $V_{Q1} < V_{RT1}$ for $t > T_{RR}$) a logic LOW signal is generated at the pin RO to reset an external microcontroller.

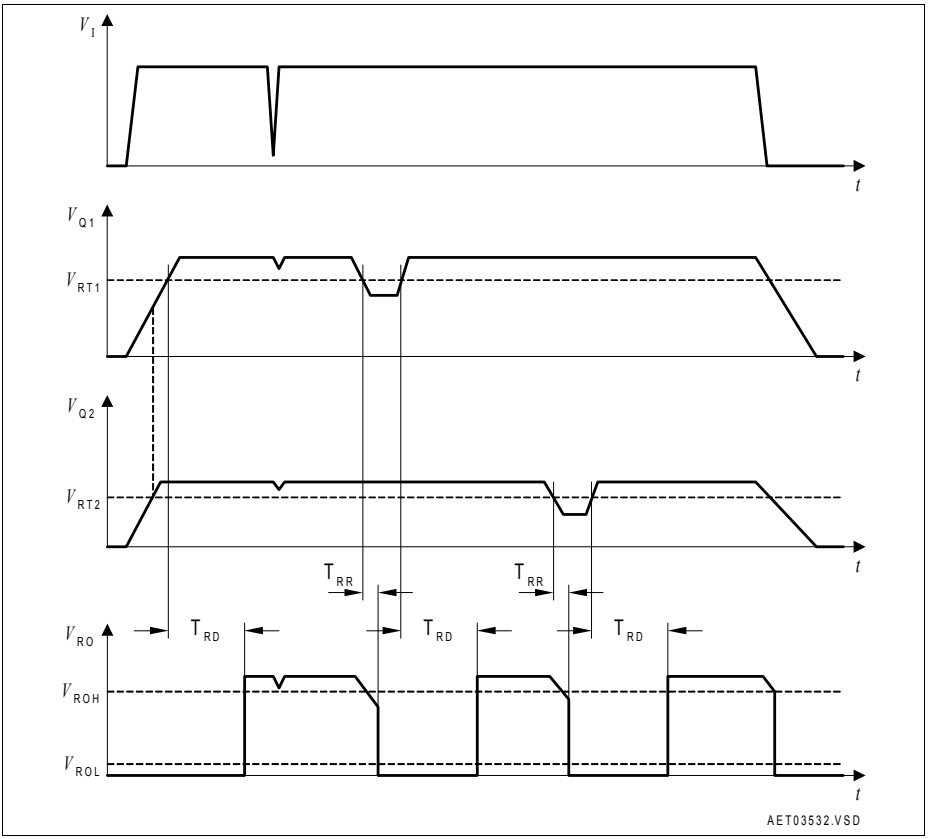


Figure 5 Reset Function and Timing Diagram

Watchdog Operation

The watchdog uses a fraction of the charge pump oscillator's clock signal as timebase. Connecting the DT pin to Q1 or to Q2 the watchdog timebase can be adjusted. The watchdog can be turned off by a low level ($V_{DT} \leq 0.8$ V) applied to the DT pin. The timing values used in this text refer to typ. values with DT connected to Q1 (fast timing).

Figure 6 shows the state diagram of the window watchdog (WWD). After power-on, the reset output signal at the RO pin (microcontroller reset) is kept LOW for the reset delay time T_{RD} of typ. 8 ms. With the LOW to HIGH transition of the signal at RO the device starts the ignore window time t_{CW} (32 ms). During this window the signal at the WDI pin is ignored. Next the WWD starts the open window. When a valid trigger signal is detected during the open window a closed window is initialized immediately. A trigger signal within

the closed window is interpreted as a pretrigger failure and results in a reset. After the closed window the open window with the duration t_{OW} is started again. The open window lasts at minimum until the trigger process has occurred, at maximum t_{OW} is 32 ms (typ. value with fast timing).

A HIGH to LOW transition of the watchdog trigger signal on pin WDI is taken as a trigger. To avoid wrong triggering due to parasitic glitches two HIGH samples followed by two LOW samples (sample period t_{sam} typ. 0.25 ms) are decoded as a valid trigger (see **Figure 7**). A reset is generated (RO goes LOW) if there is no trigger pulse during the open window or if a pretrigger occurs during the closed window. The triggering is correct also, if the first three samples (two HIGH one LOW) of the trigger pulse at pin WDI are inside the closed window and only the fourth sample (the second LOW sample) is taken in the open window.

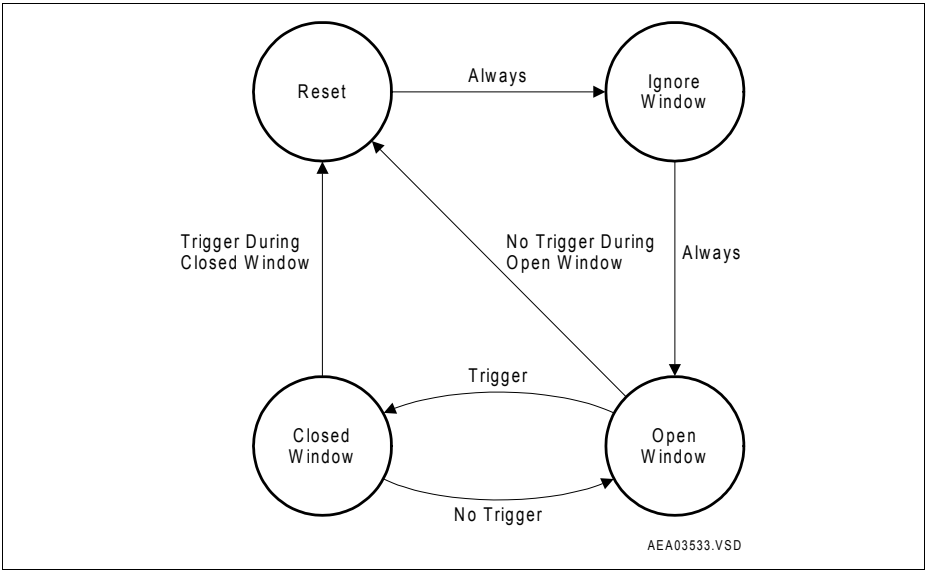


Figure 6 Window Watchdog State Diagram

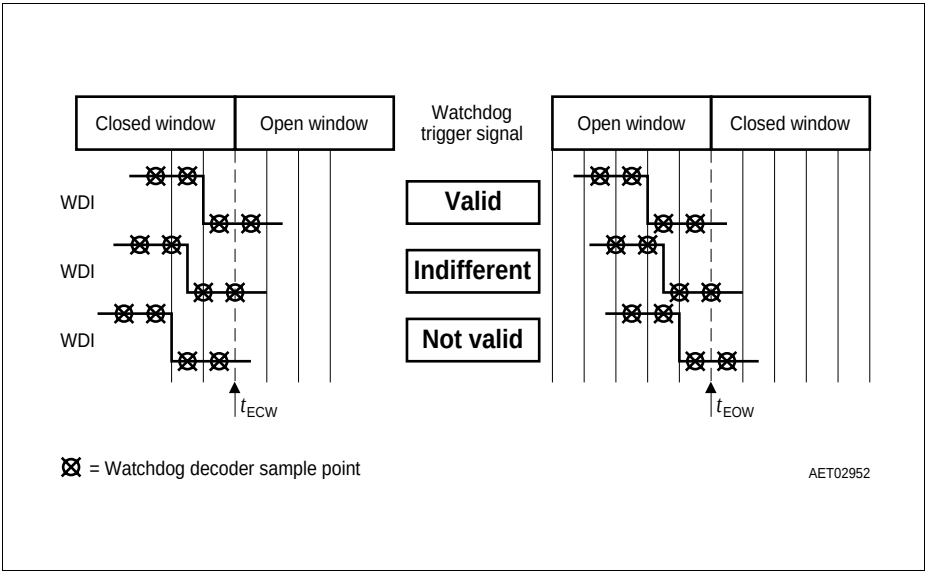


Figure 7 Window Watchdog Definitions

Package Outlines

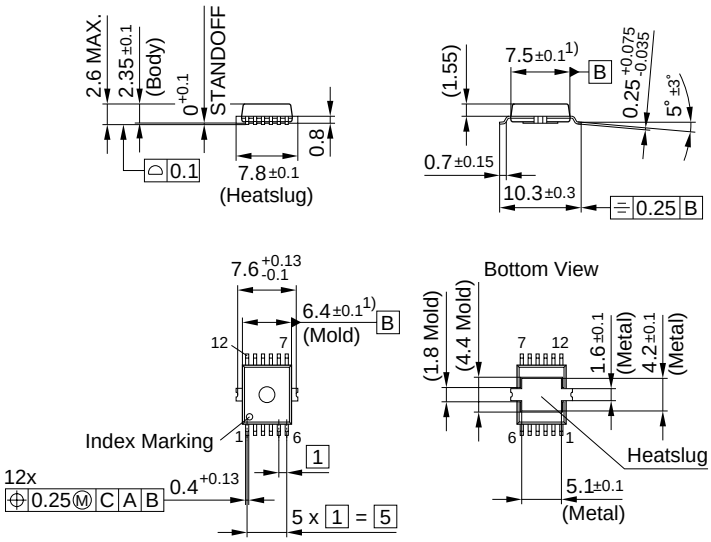


Figure 8 **P-DSO-12-4** (Plastic Dual Small Outline)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

Revision History:	**2004-10-28**	Rev. 1.3
Previous Version:	1.21	
	status final both products	

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